MCP6031/2/3/4

0.9 µA, High Precision Op Amps

Features

- Rail-to-Rail Input and Output
- Low Offset Voltage: ±150 µV (maximum)
- Ultra Low Quiescent Current: 0.9 µA (typical)
- Wide Power Supply Voltage: 1.8V to 5.5V
- Gain Bandwidth Product: 10 kHz (typical)
- Unity Gain Stable
- Chip Select ($\overline{CS}$) capability: MCP6033
- Extended Temperature Range:
  - -40°C to +125°C
- No Phase Reversal

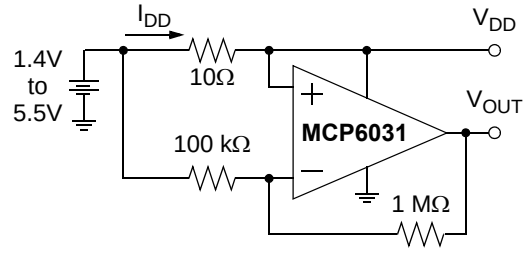
Applications

- Toll Booth Tags
- Wearable Products
- Battery Current Monitoring
- Sensor Conditioning
- Battery Powered

Design Aids

- SPICE Macro Models
- FilterLab® Software
- Mindi™ Circuit Designer & Simulator
- MAPS (Microchip Advanced Part Selector)
- Analog Demonstration and Evaluation Boards
- Application Notes

Typical Application



$$I_{DD} = \frac{V_{DD} - V_{OUT}}{(10\ V/V) \cdot (10\Omega)}$$

High Side Battery Current Sensor

Description

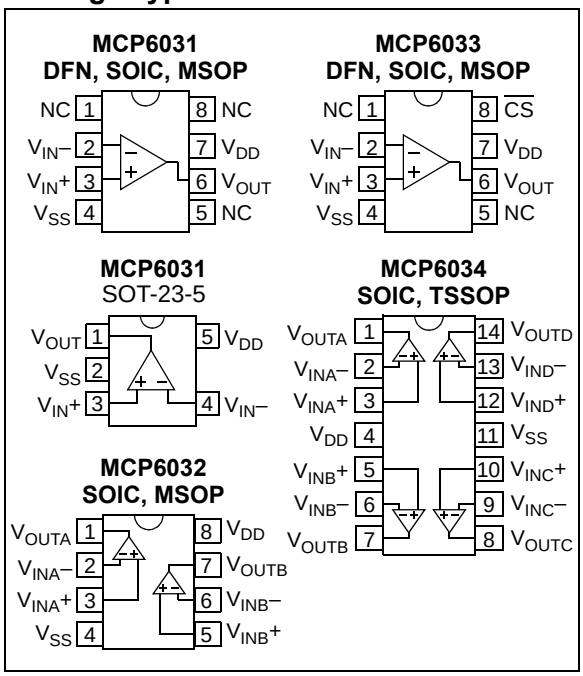
The Microchip Technology Inc. MCP6031/2/3/4 family of operational amplifiers (op amps) operate with a single supply voltage as low as 1.8V, while drawing ultra low quiescent current per amplifier (0.9 µA, typical). This family also has low input offset voltage (±150 µV, maximum) and rail-to-rail input and output operation. This combination of features supports battery-powered and portable applications.

The MCP6031/2/3/4 family is unity gain stable and has a gain bandwidth product of 10 kHz (typical). These specs make these op amps appropriate for low frequency applications, such as battery current monitoring and sensor conditioning.

The MCP6031/2/3/4 family is offered in single (MCP6031), single with power saving Chip Select ($\overline{CS}$) input (MCP6033), dual (MCP6032), and quad (MCP6034) configurations.

The MCP6031/2/3/4 family is designed with Microchip's advanced CMOS process. All devices are available in the extended temperature range, with a power supply range of 1.8V to 5.5V.

Package Types



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 7.0V
Current at Input Pins .....±2 mA
Analog Inputs ($V_{IN}+$, $V_{IN}-$)†† ..... V_{SS} – 1.0V to V_{DD} + 1.0V
All Other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage ..... $|V_{DD} - V_{SS}|$
Output Short-Circuit Current .....continuous
Current at Output and Supply Pins .....±30 mA
Storage Temperature.....-65°C to +150°C
Maximum Junction Temperature (T_J) ..... +150°C
ESD protection on all pins (HBM; MM) ..... ≥ 4 kV; 400V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See 4.1.2 "Input Voltage And Current Limits"

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS}=GND, T_A= +25°C, V_{CM} = $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 1 MΩ to V_L and $\overline{CS}$ is tied low. (Refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-150	—	+150	µV	V_{DD} = 3.0V, V_{CM} = $V_{DD}/3$
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±3.0	—	µV/°C	T_A= -40°C to +125°C, V_{DD} = 3.0V, V_{CM} = $V_{DD}/3$
Power Supply Rejection Ratio	PSRR	70	88	—	dB	V_{CM} = V_{SS}
Input Bias Current and Impedance						
Input Bias Current	I_B	—	±1.0	100	pA	
	I_B	—	60	—	pA	T_A = +85°C
	I_B	—	2000	5000	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	±1.0	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||6	—	Ω||pF	
Common Mode						
Common Mode Input Voltage Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} + 0.3	V	
Common Mode Rejection Ratio	CMRR	70	95	—	dB	V_{CM} = -0.3V to 2.1V, V_{DD} = 1.8V
		72	93	—	dB	V_{CM} = -0.3V to 5.8V, V_{DD} = 5.5V
		70	89	—	dB	V_{CM} = 2.75V to 5.8V, V_{DD} = 5.5V
		72	93	—	dB	V_{CM} = -0.3V to 2.75V, V_{DD} = 5.5V
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	95	115	—	dB	0.2V < V_{OUT} < (V_{DD} – 0.2V) R_L = 50 kΩ to V_L

DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS}=GND, T_A= +25°C, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L and $\overline{CS}$ is tied low. (Refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 10	—	V_{DD} – 10	mV	R_L = 50 kΩ to V_L, 0.5V input overdrive
Output Short-Circuit Current	I_{SC}	—	±5	—	mA	V_{DD} = 1.8V
		—	±23	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per Amplifier	I_Q	0.4	0.9	1.35	µA	I_O = 0, V_{CM} = V_{DD}, V_{DD} = 5.5V

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +1.8 to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, C_L = 60 pF, R_L = 1 MΩ to V_L and $\overline{CS}$ is tied low. (Refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	10	—	kHz	
Phase Margin	PM	—	65	—	°	G = +1 V/V
Slew Rate	SR	—	4.0	—	V/ms	
Noise						
Input Noise Voltage	E_{ni}	—	3.9	—	µVp-p	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	165	—	nV/√Hz	f = 1 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz

MCP6033 CHIP SELECT ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} =GND, T_A = +25°C, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, C_L = 60 pF, R_L = 1 MΩ to V_L and $\overline{CS}$ is tied low (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2V_{DD}	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	—	-10	—	pA	$\overline{CS}$ = V_{SS}
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	0.8V_{DD}		V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	10	—	pA	$\overline{CS}$ = V_{DD}
GND Current	I_{SS}	—	-400	—	pA	$\overline{CS}$ = V_{DD}
Amplifier Output Leakage	$I_{O(LEAK)}$	—	10	—	pA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Dynamic Specifications						
$\overline{CS}$ Low to Amplifier Output Turn-on Time	t_{ON}	—	4	100	ms	$\overline{CS}$ ≤ 0.2V_{DD} to V_{OUT} = 0.9V_{DD}/2, G = +1 V/V, V_{IN} = V_{DD}/2, R_L = 50 kΩ to V_L = V_{SS}.
$\overline{CS}$ High to Amplifier Output High-Z	t_{OFF}	—	10	—	µs	$\overline{CS}$ ≥ 0.8V_{DD} to V_{OUT} = 0.1V_{DD}/2, G = +1 V/V, V_{IN} = V_{DD}/2, R_L = 50 kΩ to V_L = V_{SS}.
$\overline{CS}$ Hysteresis	V_{HYST}	—	0.3V_{DD}	—	V	

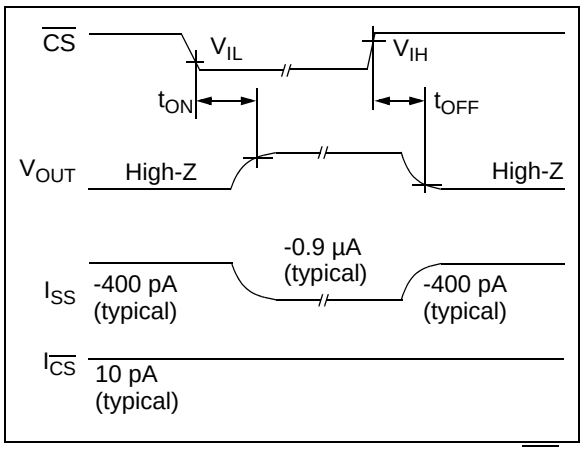


FIGURE 1-1: *Timing Diagram for the $\overline{CS}$ Pin on the MCP6033.*

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V and V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	**Note**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 8L-DFN (2x3)	θ_{JA}	—	84	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +150°C.

1.1 Test Circuits

The test circuits used for the DC and AC tests are shown in Figure 1-2 and Figure 1-3. The bypass capacitors are laid out according to the rules discussed in **Section 4.6 "Supply Bypass"**.

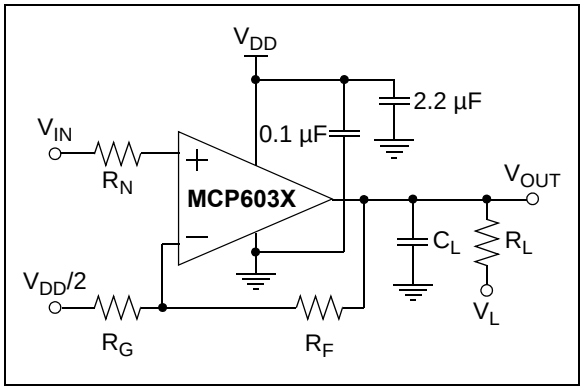


FIGURE 1-2: *AC and DC Test Circuit for Most Non-Inverting Gain Conditions.*

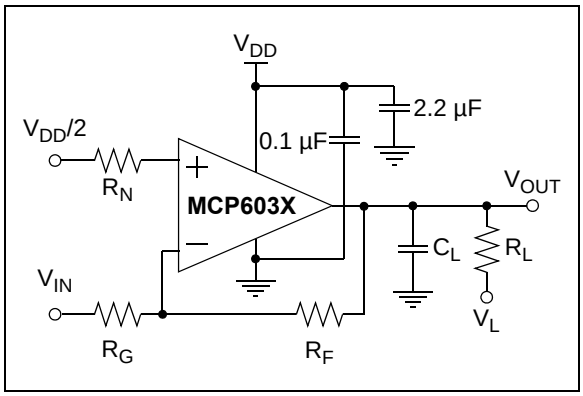
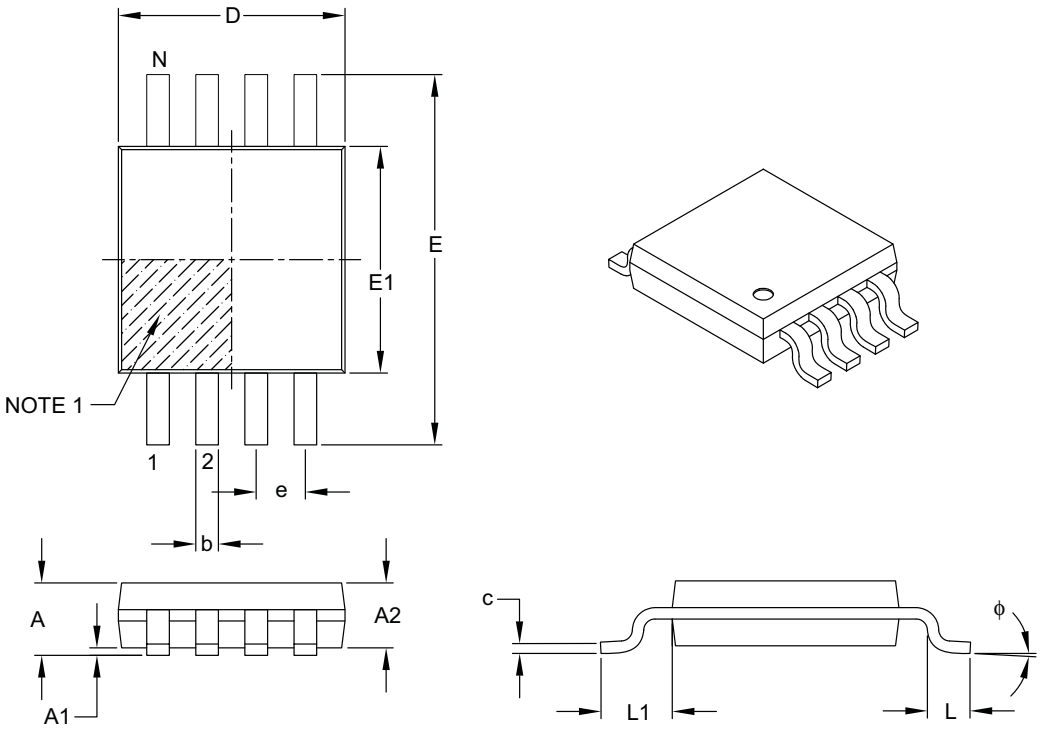


FIGURE 1-3: *AC and DC Test Circuit for Most Inverting Gain Conditions.*

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP6031:	Single Op Amp
	MCP6031T:	Single Op Amp (Tape and Reel)
	MCP6032:	Dual Op Amp
	MCP6032T:	Dual Op Amp (Tape and Reel)
	MCP6033:	Single Op Amp with Chip Select
	MCP6033T:	Single Op Amp with Chip Select (Tape and Reel)
	MCP6034:	Quad Op Amp
	MCP6034T:	Quad Op Amp (Tape and Reel)
Temperature Range:	E =	-40°C to +125°C
Package:	MC =	Plastic Dual Flat, No Lead, (2x3 DFN) 8-lead **
	MS =	Plastic MSOP, 8-lead
	OT =	Plastic Small Outline Transistor, 5-lead *
	SL =	Plastic SOIC (150 mil Body), 14-lead
	SN =	Plastic SOIC, (150 mil Body), 8-lead
	ST =	Plastic TSSOP (4.4mm Body), 14-lead

* This package is only available on the MCP6031 device.
** These packages are only available on the MCP6031 and MCP6033 devices.

Examples:

a)	MCP6031-E/SN:	8LD SOIC package.
b)	MCP6031T-E/SN:	Tape and Reel, 8LD SOIC package.
c)	MCP6031-E/MS:	8LD MSOP package.
d)	MCP6031T-E/MS:	Tape and Reel, 8LD MSOP package.
e)	MCP6031-E/MC:	8LD DFN package.
f)	MCP6031T-E/MC:	Tape and Reel, 8LD DFN package.
g)	MCP6031T-E/OT:	Tape and Reel, 5-LD SOT-23 package.
a)	MCP6032-E/SN:	8LD SOIC package.
b)	MCP6032T-E/SN:	Tape and Reel, 8LD SOIC package.
c)	MCP6032-E/MS:	8LD MSOP package
d)	MCP6032T-E/MS:	Tape and Reel 8LD MSOP package.
a)	MCP6033-E/SN:	8LD SOIC package.
b)	MCP6033T-E/SN:	Tape and Reel, 8LD SOIC package.
c)	MCP6033-E/MS:	8LD MSOP package.
d)	MCP6033T-E/MS:	Tape and Reel, 8LD MSOP package.
e)	MCP6033-E/MC:	8LD DFN package.
f)	MCP6033T-E/MC:	Tape and Reel, 8LD DFN package.
a)	MCP6034-E/SL:	14LD SOIC package.
b)	MCP6034T-E/SL:	Tape and Reel, 14LD SOIC package.
c)	MCP6034-E/ST:	14LD TSSOP package.
d)	MCP6034T-E/ST:	Tape and Reel, 14LD TSSOP package.